Dual High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Dual Outputs: 3.3V and 5V or User Programmable**
- **Ultrahigh Efficiency: Over 95% Possible**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained over 3 Decades of Output Current
- Low Standby Current at Light Loads: 160µA/Output
- Independent Micropower Shutdown: I_Q < 40µA
- Wide V_{IN} Range: 3.5V to 20V
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Available in Standard 28-Pin SSOP

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC®1142/LTC1142L/LTC1142HV are dual synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. The devices are composed of two separate regulator blocks, each driving a pair of external complementary power MOSFETs, at switching frequencies up to 250kHz, using a constant off-time current mode architecture providing constant ripple current in the inductor.

The operating current level for both regulators is user programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V* to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1142 series is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

TYPICAL APPLICATION

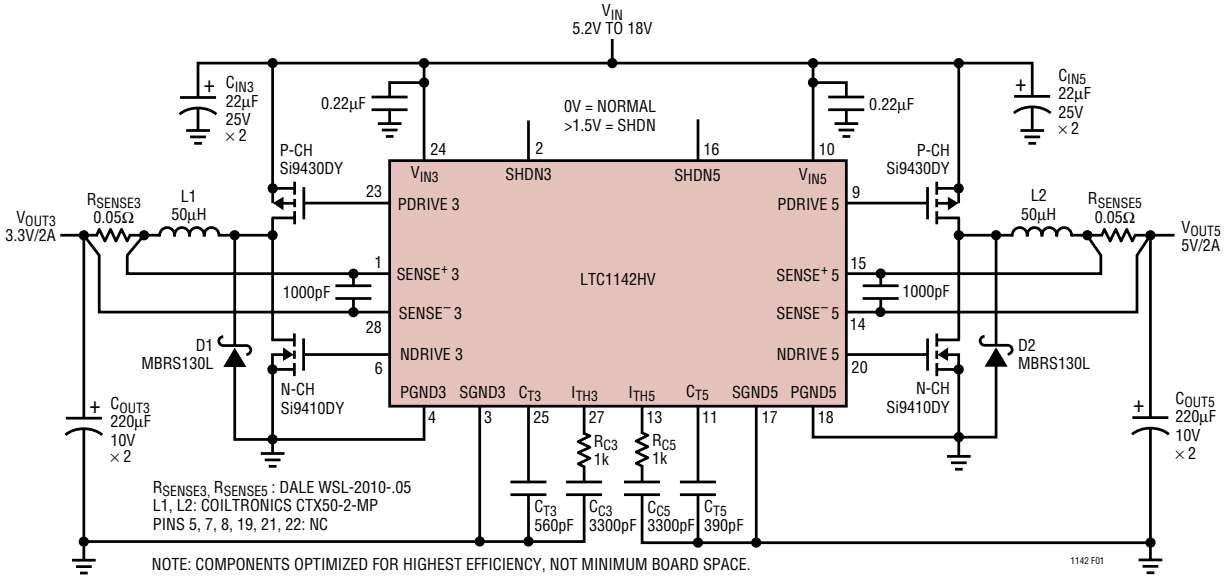


Figure 1. High Efficiency Dual 3.3V, 5V Supply

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (Pins 10, 24)
- LTC1142, LTC1142L-ADJ ..... 16V to –0.3V
- LTC1142HV, LTC1142HV-ADJ ..... 20V to –0.3V

Continuous Output Current (Pins 6, 9, 20, 23) 50mA

Sense Voltages (Pins 1, 14, 15, 28)
- V_{IN} > 13V ..... 13V to –0.3V
- V_{IN} < 13V ..... (V_{IN} + 0.3V) to –0.3V

Operating Ambient Temperature Range ..... 0°C to 70°C

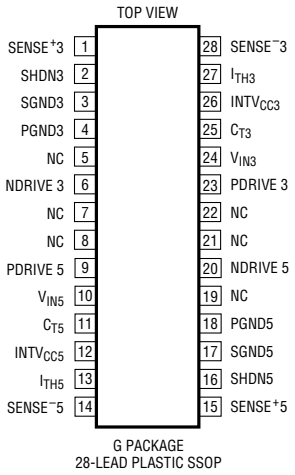
Extended Commercial
- Temperature Range ..... –40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

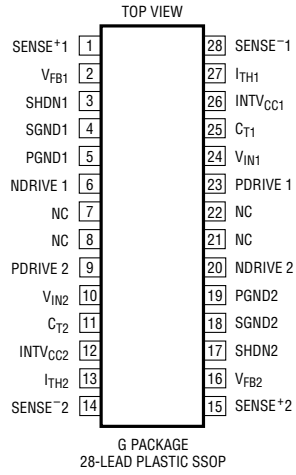


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1142CG
LTC1142HVCG



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1142HVCG-ADJ
LTC1142LCG-ADJ

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{10} = V_{24} = 10V, V_{SHDN} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_2, V_{16}	Feedback Voltage	LTC1142HV-ADJ, LTC1142L-ADJ : V_{10}, V_{24} = 9V	●	1.21	1.25	1.29	V
I_2, I_{16}	Feedback Current	LTC1142HV-ADJ, LTC1142L-ADJ	●		0.2	1	µA
V_{OUT}	Regulated Output Voltage	LTC1142, LTC1142HV					
	3.3V Output	I_{LOAD} = 700mA, V_{24} = 9V	●	3.23	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA, V_{10} = 9V	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{10}, V_{24} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation	Figure 1 Circuit					
	3.3V Output	5mA < I_{LOAD} < 2A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2A	●		60	100	mV
	Output Ripple (Burst Mode)	I_{LOAD} = 0A			50		mV_{P-P}
I_{10}, I_{24}	Input DC Supply Current (Note 3)	LTC1142					
	Normal Mode	4V < V_{10}, V_{24} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{24} < 12V, 6V < V_{10} < 12V			160	230	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 4V < V_{10}, V_{24} < 12V			10	20	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{10} = V_{24} = 10V, V_{SHDN} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input DC Supply Current (Note 3)	LTC1142HV, LTC1142HV-ADJ					
	Normal Mode	4V < V_{10}, V_{24} < 18V			1.6	2.3	mA
	Sleep Mode	4V < V_{24} < 18V, 6V < V_{10} < 18V			160	250	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 4V < V_{10}, V_{24} < 18V			10	22	µA
	Input DC Supply Current (Note 3)	LTC1142L-ADJ (Note 6)					
	Normal Mode	3.5V < V_{10}, V_{24} < 12V			1.6	2.1	mA
	Sleep Mode	3.5V < V_{10}, V_{24} < 12V			160	230	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 3.5V < V_{10}, V_{24} < 12V			10	20	µA
$V_1 - V_{28}$ $V_{15} - V_{14}$	Current Sense Threshold Voltage	LTC1142HV-ADJ, LTC1142L-ADJ					
		V_{14} = V_{28} = V_{OUT} + 100mV, V_2 = V_{16} = V_{REF} + 25mV			25		mV
		V_{14} = V_{28} = V_{OUT} – 100mV, V_2 = V_{16} = V_{REF} – 25mV	●	130	150	170	mV
		LTC1142, LTC1142HV					
		V_{28} = V_{OUT} + 100mV (Forced)			25		mV
		V_{28} = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
		LTC1142, LTC1142HV					
		V_{14} = V_{OUT} + 100mV (Forced)			25		mV
		V_{14} = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
V_{SHDN}	Shutdown Pin Threshold			0.5	0.8	2	V
I_{SHDN}	Shutdown Pin Input Current	0V < V_{SHDN} < 8V, V_{10}, V_{24} = 16V			1.2	5	µA
I_{11}, I_{24}	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 6, 9, 20, 23), V_{10}, V_{24} = 6V			100	200	ns

–40°C ≤ T_A ≤ 85°C (Note 5), V_{10} = V_{24} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_2, V_{16}	Feedback Voltage	LTC1142HV-ADJ Only: V_{10}, V_{24} = 9V	1.21	1.25	1.29	V
I_2, I_{16}	Feedback Current	LTC1142HV-ADJ Only		0.2	1	µA
V_{OUT}	Regulated Output Voltage	LTC1142, LTC1142HV				
	3.3V Output	I_{LOAD} = 700mA, V_{24} = 9V	3.17	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA, V_{10} = 9V	4.85	5.05	5.20	V
I_{10}, I_{24}	Input DC Supply Current (Note 3)	LTC1142				
	Normal Mode	4V < V_{10}, V_{24} < 12V		1.6	2.4	mA
	Sleep Mode	4V < V_{24} < 12V, 6V < V_{10} < 12V		160	260	µA
	Shutdown	V_{SHDN} = 2.1V, 4V < V_{10}, V_{24} < 12V		10	22	µA
	Input DC Supply Current (Note 3)	LTC1142HV-ADJ, LTC1142HV				
	Normal Mode	4V < V_{10}, V_{24} < 18V		1.6	2.6	mA
	Sleep Mode	4V < V_{24} < 18V, 6V < V_{10} < 18V		160	280	µA
	Shutdown	V_{SHDN} = 2.1V, 4V < V_{10}, V_{24} < 12V		10	24	µA
	Input DC Supply Current (Note 3)	LTC1142L-ADJ (Note 6)				
	Normal Mode	3.5V < V_{10}, V_{24} < 12V		1.6	2.4	mA
	Sleep Mode	3.5V < V_{10}, V_{24} < 12V		160	260	µA
	Shutdown	V_{SD1} = V_{SD2} = 2.1V, 3.5V < V_{10}, V_{24} < 12V		10	22	µA
$V_1 - V_{28}$ $V_{15} - V_{14}$	Current Sense Threshold Voltage	LTC1142HV-ADJ, LTC1142L-ADJ				
		V_{14} = V_{28} = V_{OUT} + 100mV, V_2 = V_{16} = V_{REF} + 25mV		25		mV
		V_{14} = V_{28} = V_{OUT} – 100mV, V_2 = V_{16} = V_{REF} – 25mV	125	150	175	mV
		LTC1142, LTC1142HV				
		V_{28} = V_{OUT} + 100mV (Forced)		25		mV
		V_{28} = V_{OUT} – 100mV (Forced)	125	150	175	mV

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$ (Note 5), $V_{10} = V_{24} = 10V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		LTC1142, LTC1142HV				
		$V_{14} = V_{OUT} + 100mV$ (Forced)		25		mV
		$V_{14} = V_{OUT} - 100mV$ (Forced)	125	150	175	mV
V_{SHDN}	Shutdown Pin Threshold		0.55	0.8	2	V
t_{OFF}	Off-Time (Note 4)	$C_T = 390pF$, $I_{LOAD} = 700mA$	3.8	5	6	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1142CG: $T_J = T_A + (P_D \times 95°C/W)$

Note 3: This current is for one regulator block. Total supply current is the sum of Pins 10 and 24 currents. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

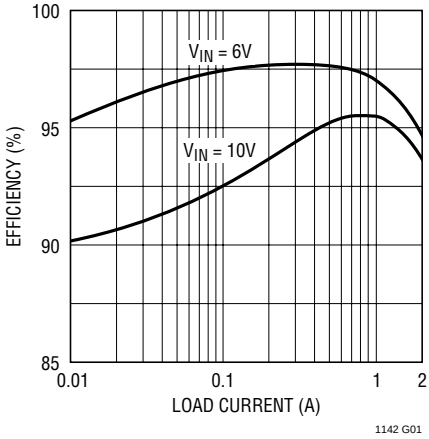
Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 5: The LTC1142/LTC1142L/LTC1142HV are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I-grade parts are available, consult the factory.

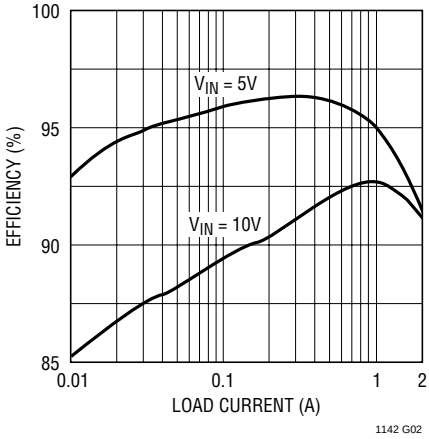
Note 6: The LTC1142L-ADJ allows operation down to $V_{IN} = 3.5V$.

TYPICAL PERFORMANCE CHARACTERISTICS

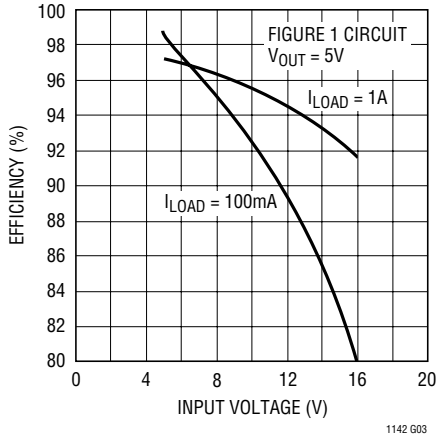
5V Output Efficiency



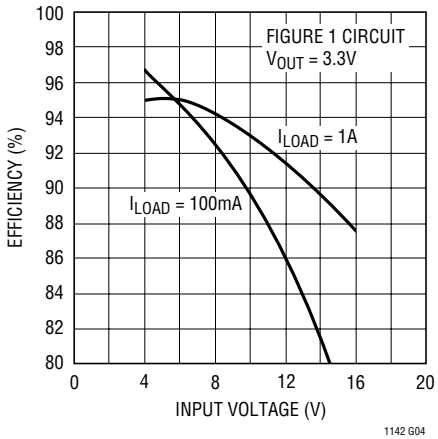
3.3V Output Efficiency



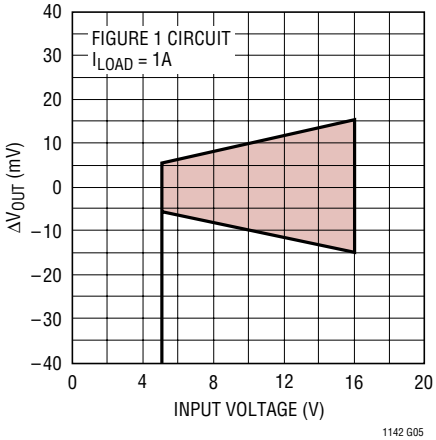
5V Efficiency vs Input Voltage



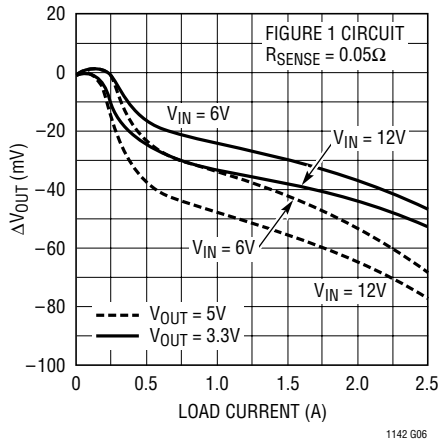
3.3V Efficiency vs Input Voltage



Line Regulation

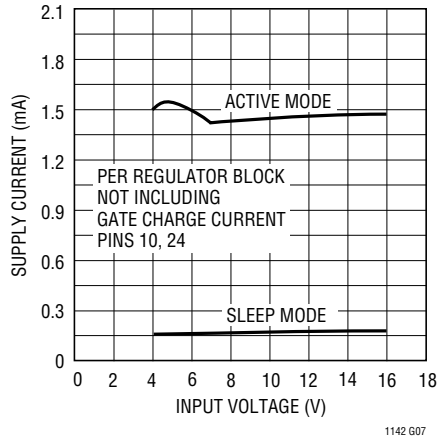


Load Regulation

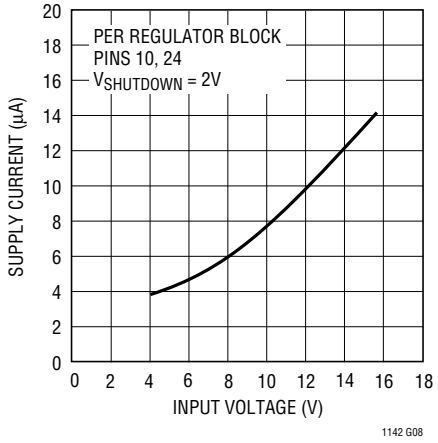


TYPICAL PERFORMANCE CHARACTERISTICS

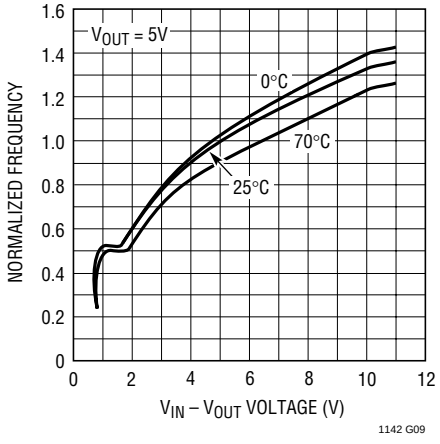
DC Supply Current



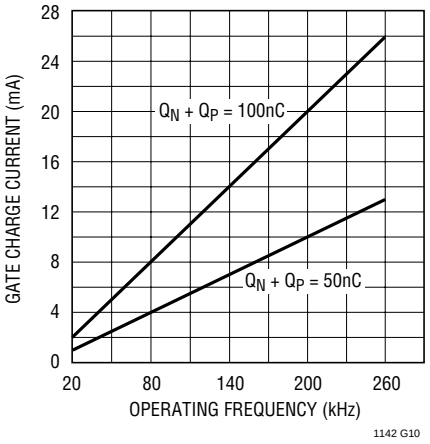
Supply Current in Shutdown



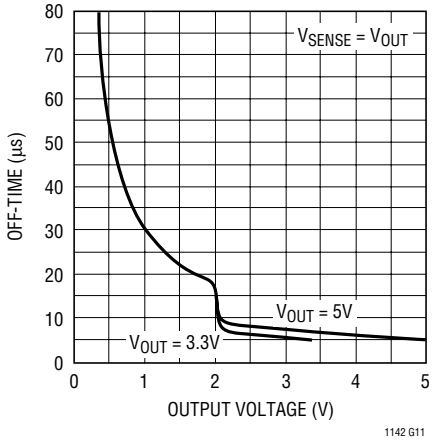
Operating Frequency vs $V_{IN} - V_{OUT}$



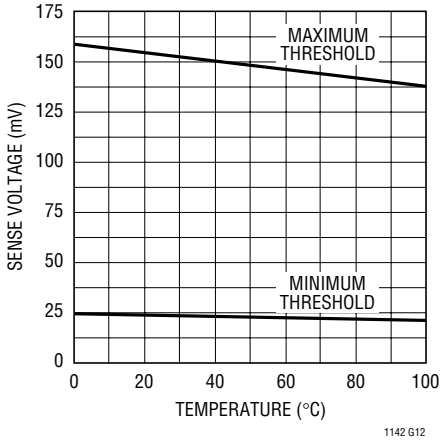
Gate Charge Supply Current



Off-Time vs Output Voltage



Current Sense Threshold Voltage



PIN FUNCTIONS

LTC1142/LTC1142HV

SENSE+3 (Pin 1): The (+) Input to the 3.3V Section Current Comparator. A built-in offset between Pins 1 and 28 in conjunction with R_{SENSE3} sets the current trip threshold for the 3.3V section.

SHDN3 (Pin 2): When grounded, the 3.3V section operates normally. Pulling Pin 2 high holds both MOSFETs off and puts the 3.3V section in micropower shutdown mode. Requires CMOS logic-level signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 2.

SGND3 (Pin 3): The 3.3V section small-signal ground must be routed separately from other grounds to the (–) terminal of the 3.3V section output capacitor.

PGND3 (Pin 4): The 3.3V section driver power ground connects to source of N-channel MOSFET and the (–) terminal of the 3.3V section input capacitor.

NC (Pin 5): No Connection.

NDRIVE3 (Pin 6): High Current Drive for Bottom N-Channel MOSFET, 3.3V Section. Voltage swing at Pin 6 is from ground to V_{IN3}.

PIN FUNCTIONS

NC (Pins 7, 8): No Connection.

PDRIVE 5 (Pin 9): High Current Drive for Top P-Channel MOSFET, 5V Section. Voltage swing at this pin is from V_{IN5} to ground.

V_{IN5} (Pin 10): Supply pin, 5V section, must be closely decoupled to 5V power ground Pin 18.

C_{T5} (Pin 11): External capacitor C_{T5} from Pin 11 to ground sets the operating frequency for the 5V section. (The actual frequency is also dependent upon the input voltage.)

$INTV_{CC5}$ (Pin 12) : Internal supply voltage for the 5V section, nominally 3.3V, can be decoupled to signal ground, Pin 17. Do not externally load this pin.

I_{TH5} (Pin 13): Gain Amplifier Decoupling Point, 5V Section. The 5V section current comparator threshold increases with the Pin 13 voltage.

$SENSE^-5$ (Pin 14): Connects to internal resistive divider which sets the output voltage for the 5V section. Pin 14 is also the (–) input for the current comparator on the 5V section.

$SENSE^+5$ (Pin 15): The (+) Input to the 5V Section Current Comparator. A built-in offset between Pins 15 and 14 in conjunction with R_{SENSE5} sets the current trip threshold for the 5V section.

SHDN5 (Pin 16): When grounded, the 5V section operates normally. Pulling Pin 16 high holds both MOSFETs off and puts the 5V section in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 16.

SGND5 (Pin 17): The 5V section small-signal ground must be routed separately from other grounds to the (–) terminal of the 5V section output capacitor.

PGND5 (Pin 18): The 5V section driver power ground connects to source of N-channel MOSFET and the (–) terminal of the 5V section input capacitor.

NC (Pin 19): No Connection.

NDRIVE 5 (Pin 20): High Current Drive for Bottom N-Channel MOSFET, 5V Section. Voltage swing at Pin 20 is from ground to V_{IN5}.

NC (Pins 21, 22): No Connection.

PDRIVE 3 (Pin 23): High Current Drive for Top P-Channel MOSFET, 3.3V Section. Voltage swing at this pin is from V_{IN3} to ground.

V_{IN3} (Pin 24): Supply pin, 3.3V section, must be closely decoupled to 3.3V power ground, Pin 4.

C_{T3} (Pin 25): External capacitor C_{T3} from Pin 25 to ground sets the operating frequency for the 3.3V section. (The actual frequency is also dependent upon the input voltage.)

$INTV_{CC3}$ (Pin 26): Internal supply voltage for the 3.3V section, nominally 3.3V, can be decoupled to signal ground, Pin 3. Do not externally load this pin.

I_{TH3} (Pin 27): Gain Amplifier Decoupling Point, 3.3V Section. The 3.3V section current comparator threshold increases with the Pin 27 voltage.

$SENSE^-3$ (Pin 28): Connects to internal resistive divider which sets the output voltage for the 3.3V section. Pin 28 is also the (–) input for the current comparator on the 3.3V section.

LTC1142HV-ADJ/LTC1142L-ADJ

$SENSE^+1$ (Pin 1): The (+) Input to the Section 1 Current Comparator. A built-in offset between Pins 1 and 28 in conjunction with R_{SENSE1} sets the current trip threshold for this section.

V_{FB1} (Pin 2): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 1.

SHDN1 (Pin 3): When grounded, the section 1 regulator operates normally. Pulling Pin 3 high holds both MOSFETs off and puts this section in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 3.

SGND1 (Pin 4): The section 1 small-signal ground must be routed separately from other grounds to the (–) terminal of the section 1 output capacitor.

PGND1 (Pin 5): The section 1 driver power ground connects to source of N-channel MOSFET and the (–) terminal of the section 1 input capacitor.

PIN FUNCTIONS

NDRIVE 1 (Pin 6): High Current Drive for Bottom N-Channel MOSFET, Section 1. Voltage swing at Pin 6 is from ground to V_{IN1}.

NC (Pins 7, 8): No Connection.

PDRIVE 2 (Pin 9): High Current Drive for Top P-Channel MOSFET, Section 2. Voltage swing at this pin is from V_{IN2} to ground.

V_{IN2} (Pin 10): Supply pin, section 2, must be closely decoupled to section 2 power ground, Pin 19.

C_{T2} (Pin 11): External capacitor C_{T2} from Pin 11 to ground sets the operating frequency for the section 2. (The actual frequency is also dependent upon the input voltage.)

$INTV_{CC2}$ (Pin 12) : Internal supply voltage for section 2, nominally 3.3V, can be decoupled to signal ground, Pin 18. Do not externally load this pin.

I_{TH2} (Pin 13): Gain Amplifier Decoupling Point, Section 2. The section 2 current comparator threshold increases with the Pin 13 voltage.

$SENSE^-2$ (Pin 14): Connects (–) input for the current comparator on section 2.

$SENSE^+2$ (Pin 15): The (+) Input to the Section 2 Current Comparator. A built-in offset between Pins 15 and 14 in conjunction with R_{SENSE2} sets the current trip threshold for this section.

V_{FB2} (Pin 16): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 2.

SHDN2 (Pin 17): When grounded, the section 2 regulator operates normally. Pulling Pin 17 high holds both MOSFETs off and puts section 2 in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 17.

SGND2 (Pin 18): The section 2 small-signal ground must be routed separately from other grounds to the (–) terminal of the section 2 output capacitor.

PGND2 (Pin 19): The section 2 driver power ground connects to source of the N-channel MOSFET and the (–) terminal of the section 2 input capacitor.

NDRIVE 2 (Pin 20): High Current Drive for Bottom N-Channel MOSFET, Section 2. Voltage swing at Pin 20 is from ground to V_{IN2}.

NC (Pins 21, 22): No Connection.

PDRIVE 1 (Pin 23): High Current Drive for Top P-Channel MOSFET, Section 1. Voltage swing at this pin is from V_{IN1} to ground.

V_{IN1} (Pin 24): Supply Pin, Section 1. Must be closely decoupled to section 1 power ground Pin 5.

C_{T1} (Pin 25): External capacitor C_{T1} from Pin 25 to ground sets the operating frequency for section 1. (The actual frequency is also dependent upon the input voltage.)

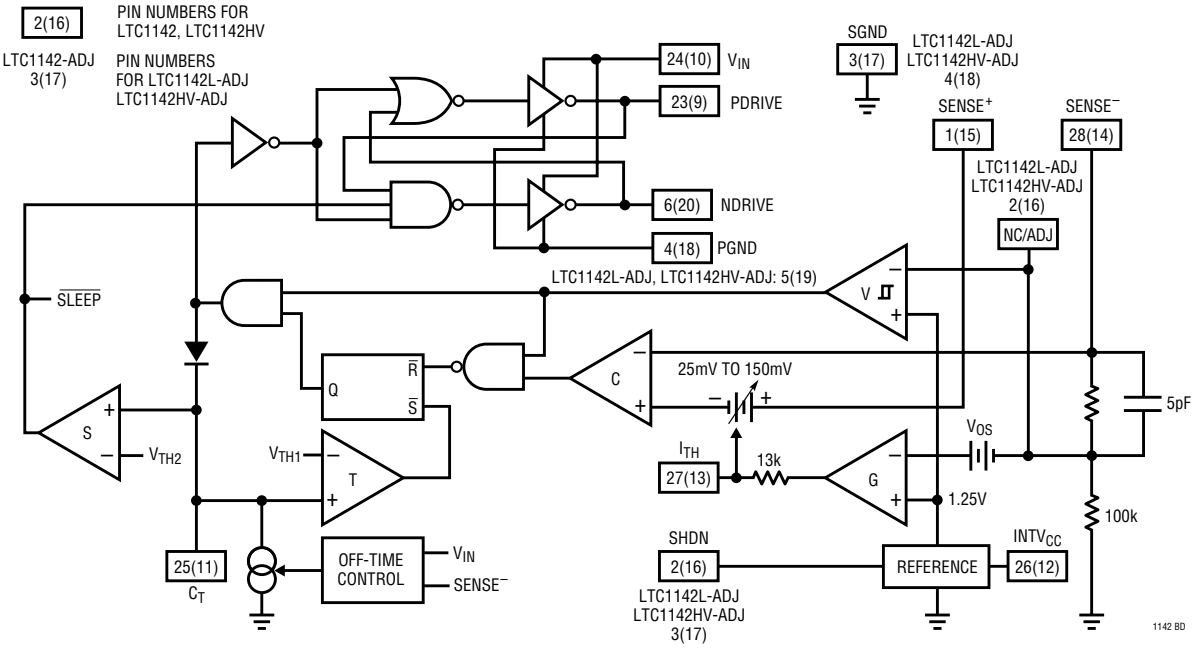
$INTV_{CC1}$ (Pin 26): Internal supply voltage for section 1, nominally 3.3V, can be decoupled to signal ground, Pin 4. Do not externally load this pin.

I_{TH1} (Pin 27): Gain Amplifier Decoupling Point, Section 1. The section 1 current comparator threshold increases with the Pin 27 voltage.

$SENSE^-1$ (Pin 28): Connects to the (–) input for the current comparator on section 1.

FUNCTIONAL DIAGRAM

Only one regulator block shown. Pin numbers are for 3.3V (5V) sections for LTC1142/LTC1142HV, and V_{OUT1} (V_{OUT2}) for LTC1142L-ADJ/LTC1142HV-ADJ.



OPERATION

Refer to Functional Diagram

The LTC1142 series consists of two individual regulator blocks, each using current mode, constant off-time architectures to synchronously switch an external pair of complementary power MOSFETs. The two regulators are internally set to provide output voltages of 3.3V and 5V for the LTC1142. The LTC1142HV-ADJ/LTC1142L-ADJ are configured to provide two user selectable output voltages, each set by external resistor dividers. Operating frequency is individually set on each section by the external capacitors at C_T, Pins 11 and 25.

The output voltage is sensed by an internal voltage divider connected to Sense$^-$, Pin 28 (14) (LTC1142) or external divider returned to V_{FB}, Pin 2 (16) (LTC1142-ADJ). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1142 series automatically switches between two modes of operation, Burst Mode and continuous mode. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Pins 1 (15) and 28 (14) connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the PDrive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to Pin 25 (11) is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage [measured by Pin 28 (14)] to model the inductor current, which decays at a rate that is also proportional to the output voltage. While the timing capacitor is discharging, the NDrive output goes to V_{IN}, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the NDrive output to go low (turning off the N-channel MOSFET) and the PDrive output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

OPERATION Refer to Functional Diagram

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage [Pin 27(13)] to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160μA (for one regulator block). The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the NDrive output can go high, the PDrive output must also be high. Likewise, the PDrive output is prevented from going low while the NDrive output is high.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle) providing low dropout operation with $V_{OUT} \sim V_{IN}$.

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The basic LTC1142 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the 3.3V and 5V sections in the LTC1142 are identical and similarly section 1 and section 2 in the LTC1142HV-ADJ/LTC1142L-ADJ are identical, the process of component selection is the same for both sections. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 20V.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1142 current comparators have a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency section). Solving for R_{SENSE} and allowing a margin for variations in the LTC1142 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for Selecting R_{SENSE} vs Maximum Output Current is given in Figure 2.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current $I_{SC(PK)}$,

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both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1142 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

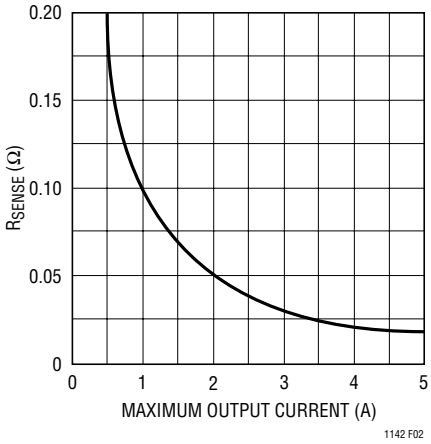

Figure 2. Selecting R_{SENSE}

L and C_T Selection for Operating Frequency

Each regulator section of the LTC1142 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{2.6 \bullet 10^4 \bullet f}$$

Assumes $V_{IN} = 2V_{OUT}$, Figure 1 circuit.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations section). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \bullet 10^4 \bullet C_T \bullet \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input-to-output voltage differential drops below 1.5V for a particular section, the LTC1142 reduces t_{OFF} in that section by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

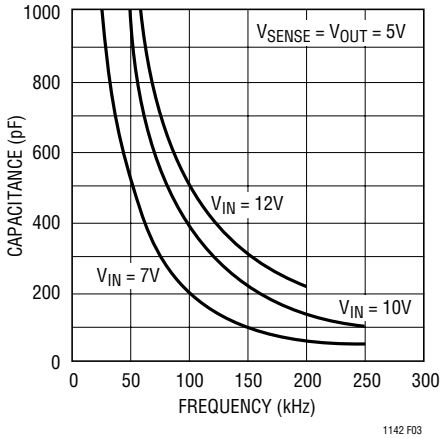

Figure 3. Timing Capacitor Value

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \bullet 10^5 \bullet R_{SENSE} \bullet C_T \bullet V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are

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eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1142 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, molypermalloy (MPP), or Kool Mμ® cores. Lower cost powdered iron cores provide suitable performance, but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies, but it is quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corporation which do not increase the height significantly.

Power MOSFET and D1, D2 Selection

Two external power MOSFETs must be selected for use with each section of the LTC1142: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on- resistance $R_{DS(ON)}$.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are strongly recommended. When logic-level MOSFETs are used, the LTC1142 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1142 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \bullet P_P}{V_{OUT} \bullet I_{MAX}^2 \bullet \left(1+\delta_P\right)}$$

$$\text{N-Ch } R_{DS(ON)} = \frac{V_{IN} \bullet P_N}{\left(V_{IN} - V_{OUT}\right) \bullet I_{MAX}^2 \bullet \left(1+\delta_N\right)}$$

where P_P and P_N are the allowable power dissipations and δ_P and δ_N are the temperature dependencies of $R_{DS(ON)}$. P_P and P_N will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.007/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diodes D1 and D2 shown in Figure 1 only conduct during the dead-time between the conduction of the respective power MOSFETs. The sole purpose of D1 and D2 is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the

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dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 and D2 are omitted). Therefore, D1 and D2 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case conditon is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on each V_{IN} line (Pins 10 and 24) for high frequency decoupling.

The selection of C_{OUT} is driven by the required Effective Series Resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1142:*

$$C_{OUT}\ \text{Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be parallel to meet the capacitance, ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1142 would normally be in continuous operation. The output remains in regulation at all times.

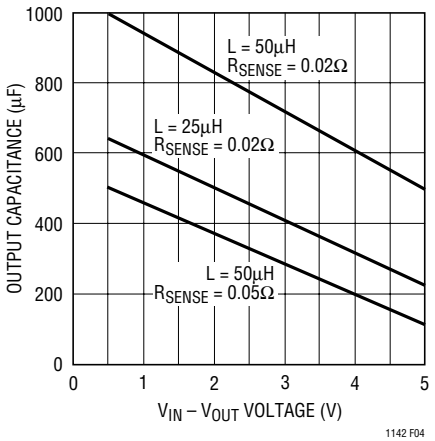

Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load

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current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady- state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 27 (13) external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1142 circuits:

1. LTC1142 DC bias current
2. MOSFET gate charge current
3. I^2R losses

1. The DC supply current is the current which flows into V_{IN} (pin 24 for the 3.3V section, Pin 10 for the 5V section) less the gate charge current. For V_{IN} = 10V the LTC1142 DC supply current for each section is 160µA with no load, and increases proportionally with load up to a constant 1.6mA after the LTC1142 has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATE(CHG)} = f (Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATE(CHG)}$ = 7.5mA in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

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Figure 5 shows how the efficiency losses in one section of a typical LTC1142 regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

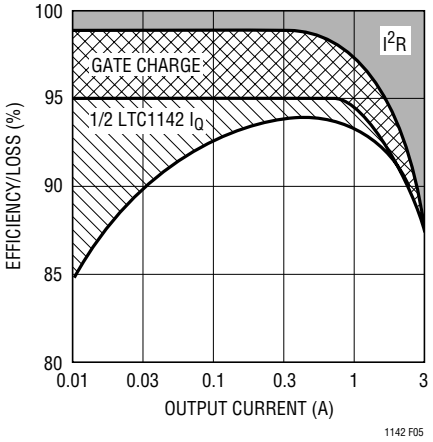

Figure 5. Efficiency Loss

Design Example

As a design example, assume V_{IN} = 12V (nominal), 5V section, I_{MAX} = 2A and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/2 = 0.05\Omega$

$t_{OFF} = (1/200kHz) \bullet [1 - (5/12)] = 2.92\mu s$

$C_{T5} = 2.92\mu s/(1.3 \bullet 10^4) = 220pF$

$L2_{MIN} = 5.1 \bullet 10^5 \bullet 0.05\Omega \bullet 220pF \bullet 5V = 28\mu H$

Assume that the MOSFET dissipations are to be limited to $P_N = P_P = 250mW$.

If T_A = 50°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = \delta_N = 0.007(63 - 25) = 0.27$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$P\text{-}Ch\ R_{DS(ON)} = \frac{12(0.25)}{5(2)^2(1.27)} = 0.12\Omega$$

$$N\text{-}Ch\ R_{DS(ON)} = \frac{12(0.25)}{5(2)^2(1.27)} = 0.085\Omega$$

The P-channel requirement can be met by a Si9430DY, while the N-channel requirement is exceeded by a Si9410DY. Note that the most stringent requirement for the N-channel MOSFET is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst case N-channel dissipation rises to:

$$P_N = I_{SC(AVG)}{}^2 \bullet R_{DS(ON)} \bullet (1 + \delta_N)$$

With the 0.05Ω sense resistor, $I_{SC(AVG)}$ = 2A will result, increasing the 0.085Ω N-channel dissipation to 450mW at a die temperature of 73°C.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V:

$$f_{MIN} = (1/2.92\mu s)[1 - (5V/7V)] = 98kHz$$

$$P_P = \frac{5V(0.12\Omega)(2A)^2(1.27)}{7V} = 435mV$$

A similar calculation for the 3.3V section results in the component values shown in Figure 14.

LTC1142HV-ADJ/LTC1142L-ADJ Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1142 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB}, Pin 2 (16). The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

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To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1142HV-ADJ/LTC1142L-ADJ as in Figure 6. The external divider network must be placed across C_{OUT} with the negative plate of C_{OUT} returned to signal ground. Refer to the Board Layout Checklist.

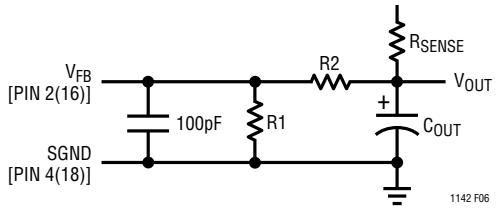

Figure 6. LTC1142-ADJ External Feedback Network

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1142. These items are also illustrated graphically in the layout diagram of Figure 7. In general each block should be self-contained with little cross coupling for best performance. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1142 signal ground [Pin 3 (17) for the LTC1142, Pin 4 (18) for LTC1142-ADJ] must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1142 Sense$^-$, Pin 28 (14) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 1 (15) and 28 (14) should be as close as possible to the LTC1142. Ensure accurate current sens-

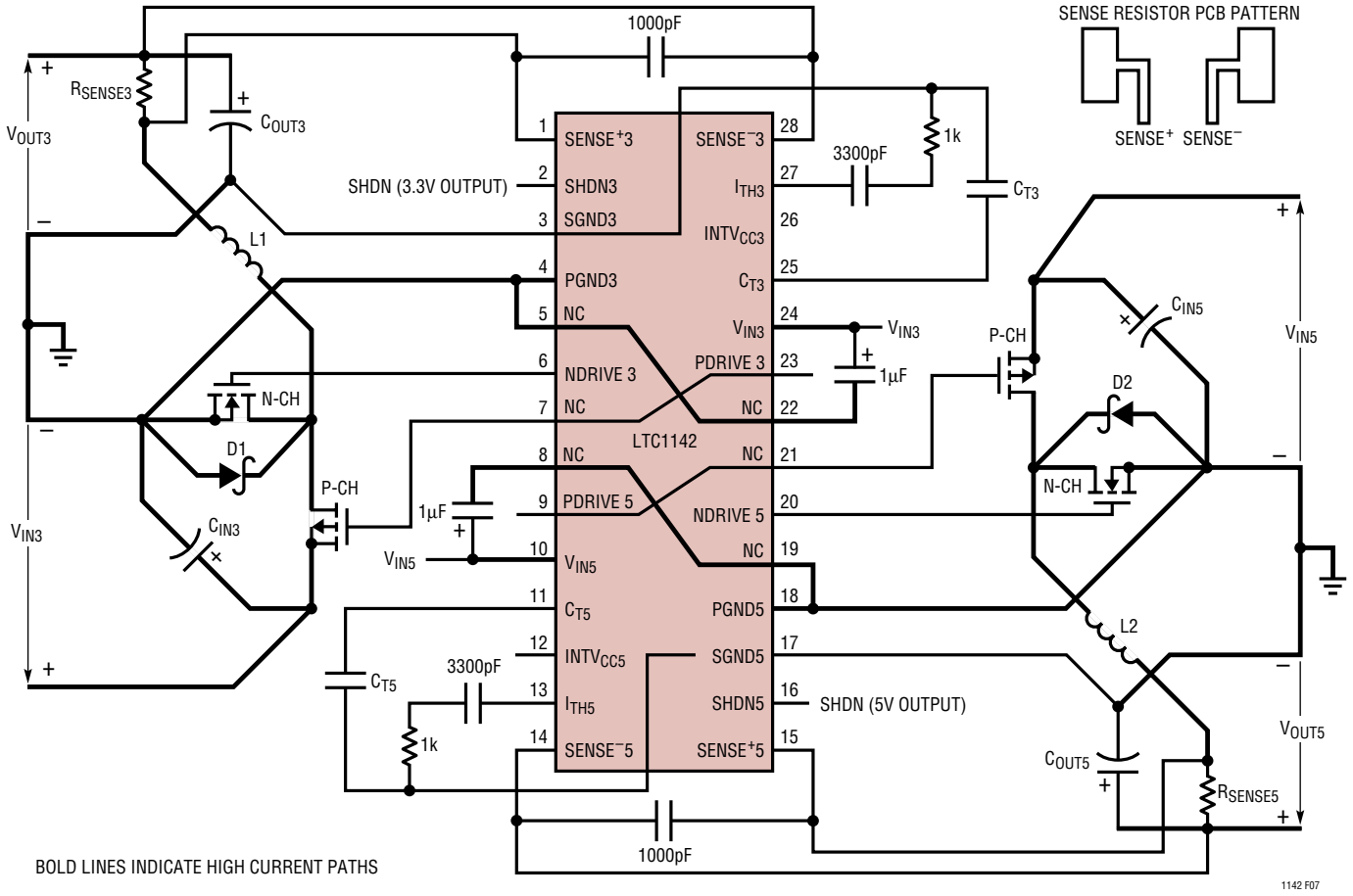

Figure 7. LTC1142 Layout Diagram (see Board Layout Checklist)

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ing with Kelvin connections. Be sure to use a PCB pattern similar to that shown in Figure 7 for the current sense resistors.

4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the input decoupling capacitor (1µF/0.22µF) connected closely between Pin 24 (10) and power ground [Pin 4 (18) for the LTC1142, Pin 5 (19) for the LTC1142-ADJ]? This capacitor carries the MOSFET driver peak currents.
6. Are the shutdown Pins 2 and 16 for the LTC1142 (Pins 3 and 17 for the LTC1142-ADJ) actively pulled to ground during normal operation? Both Shutdown pins are high impedance and must not be allowed to float. Both pins can be driven by the same external signal if needed.
7. For the LTC1142-ADJ adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the C_T , Pin 25 (11) above 1.5V when the output voltage is greater than the desired regulated value will turn "on" the N-channel MOSFET for that regulator section.

A fault condition which causes the output voltage to go above a maximum allowable value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will cause large currents to flow and blow the system fuse.

The N-channel MOSFET needs to be sized so it will safely handle this overcurrent condition. The typical delay from pulling the C_T pin high and the NDrive Pin 6 (20) going high is 250ns. Note: Under shutdown conditions, the N-channel is held OFF and pulling the C_T pin high will not cause the N-channel MOSFET to crowbar the output.

A simple N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1142 as shown in Figure 8.

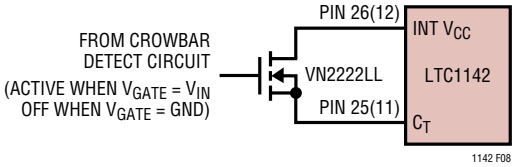


Figure 8. Output Crowbar Interface

Troubleshooting Hints

Since efficiency is critical to LTC1142 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T, Pins 25 and 11.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 9b.

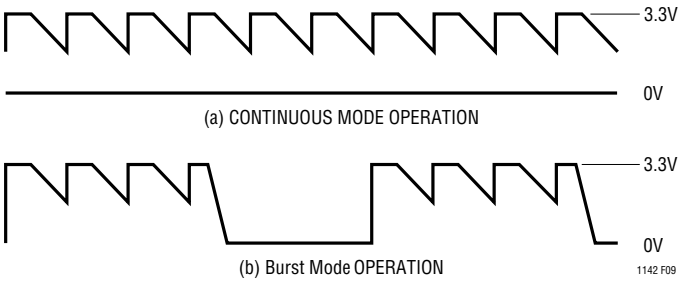


Figure 9. C_T Waveforms

Inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

If Pin 25 or Pin 11 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs

APPLICATIONS INFORMATION

may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 10. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

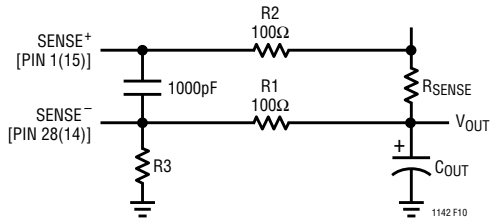


Figure 10. Suppression of Burst Mode Operation

With the addition of R3 a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \bullet \left(\frac{R1}{R1+R3} \right)$$

If V_{OFFSET} > 25mV, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Pins 1 (15) and Pins 28 (14).

TYPICAL APPLICATIONS (For additional high efficiency circuits, see Application Note 54)

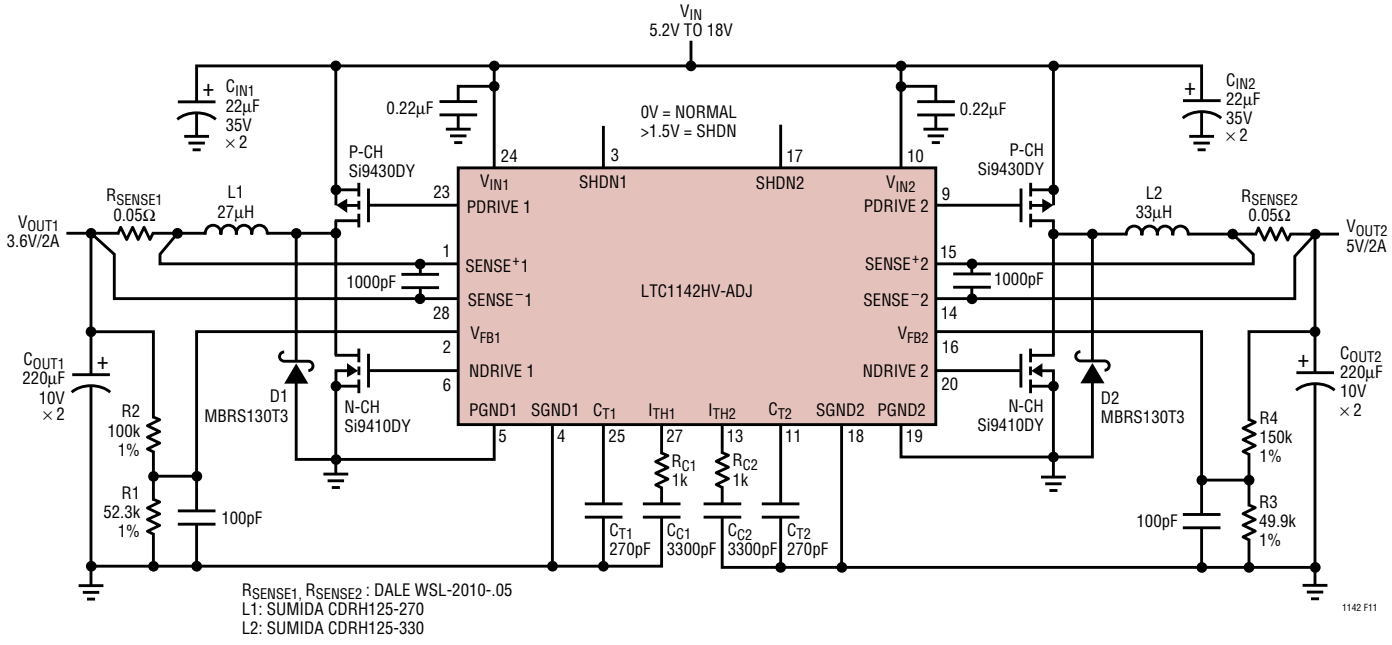


Figure 11. LTC1142HV-ADJ Dual Regulator with 3.6V/2A and 5V/2A Outputs

TYPICAL APPLICATIONS

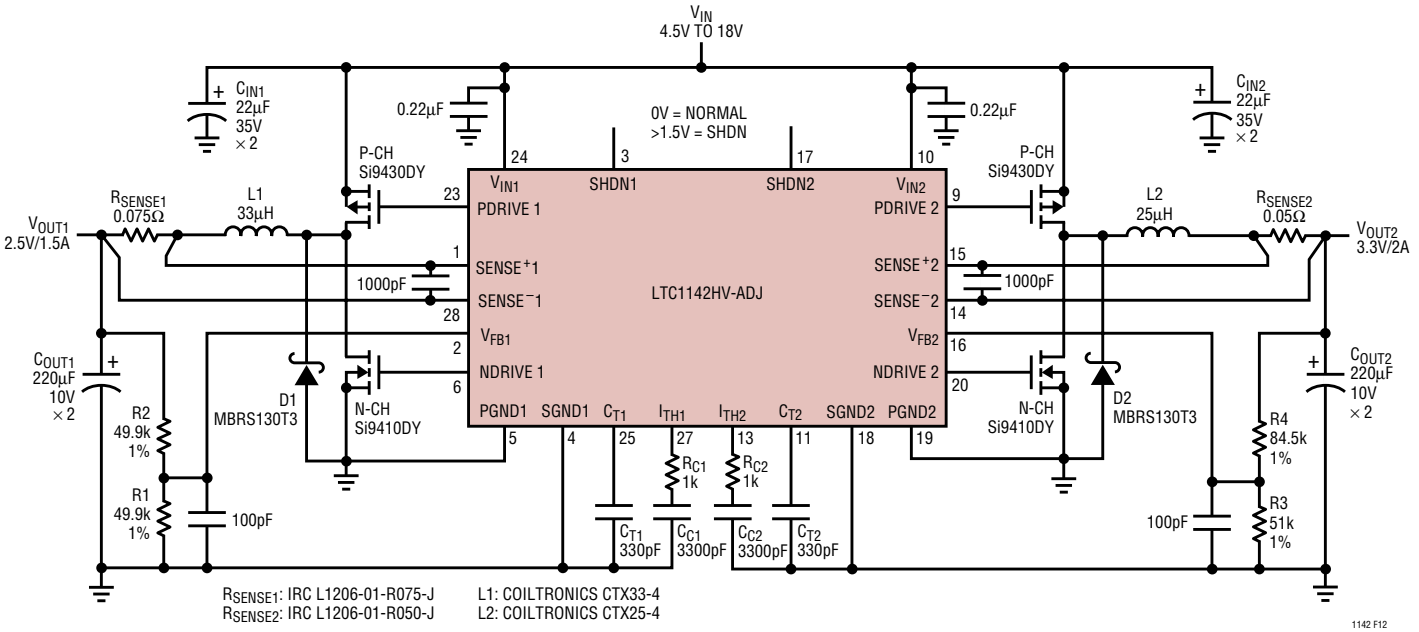


Figure 12. LTC1142HV-ADJ High Efficiency Regulator with 3.3V/2A and 2.5V/1.5A Outputs

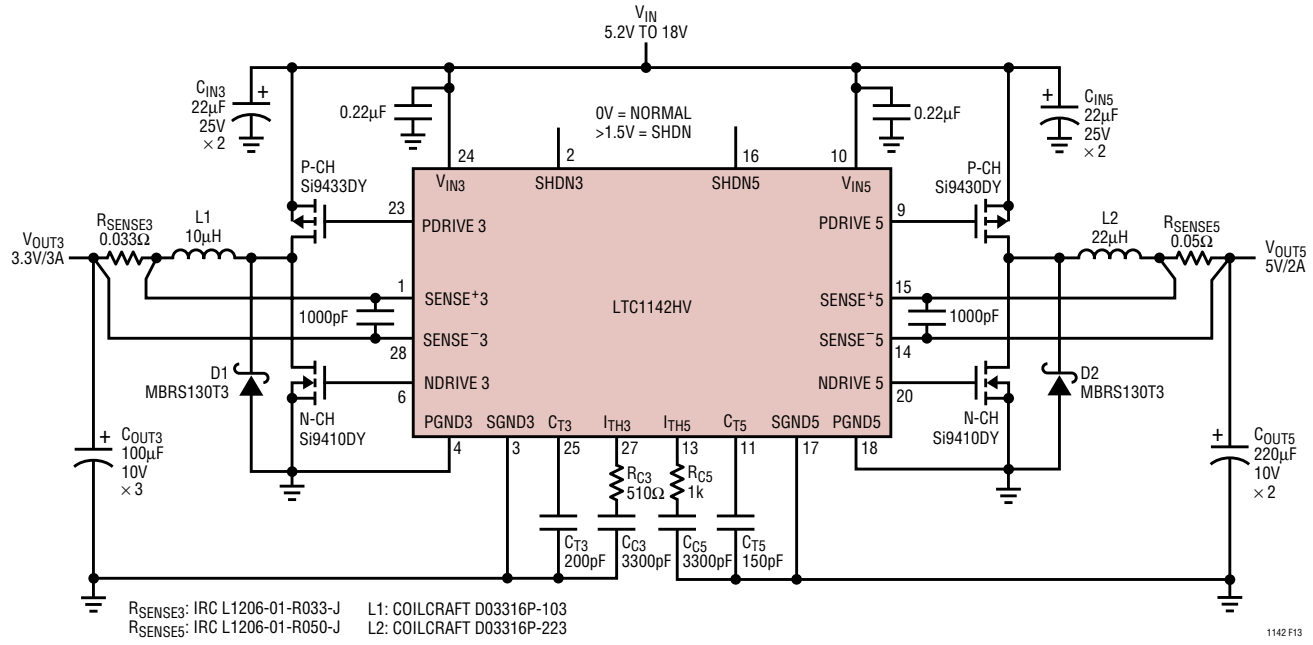


Figure 13. LTC1142HV High Efficiency Regulator with 3.3V/3A and 5V/2A Outputs

TYPICAL APPLICATIONS

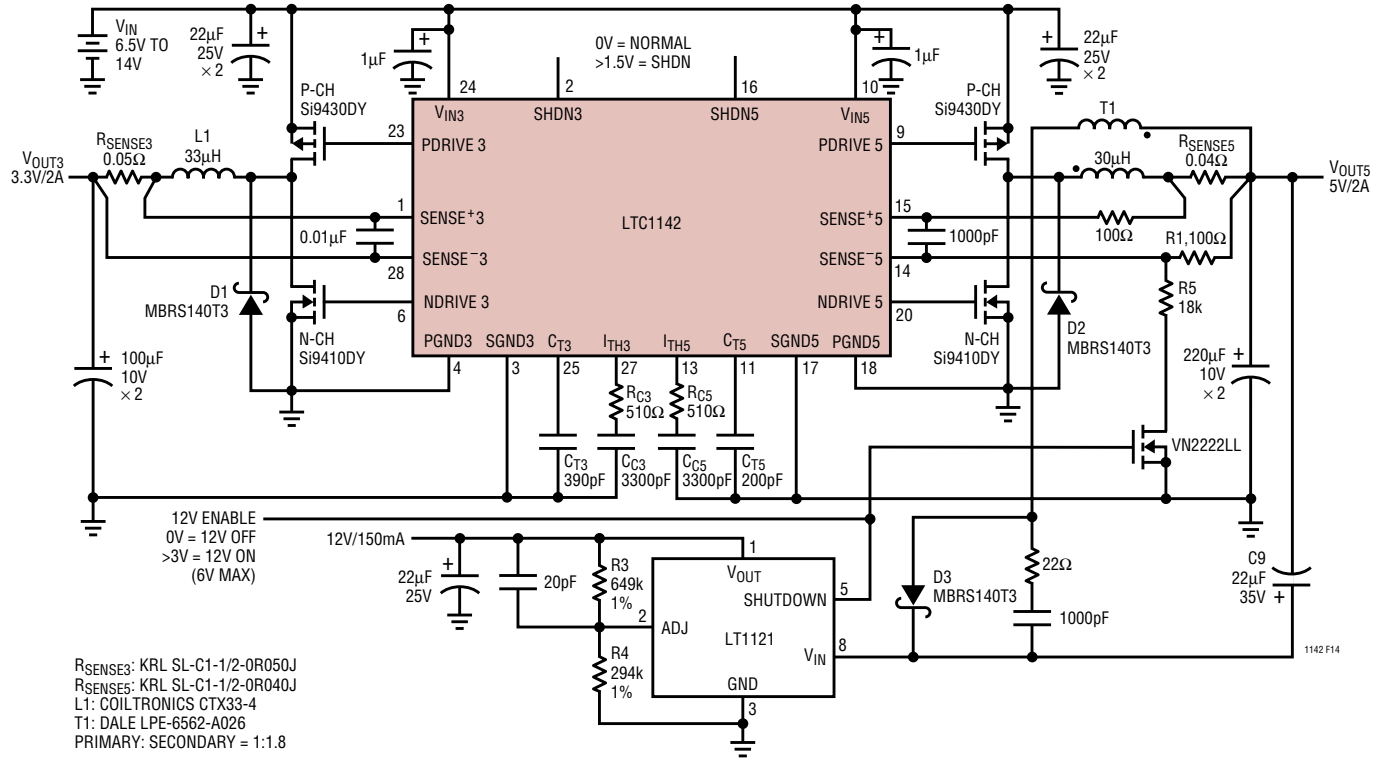


Figure 14. LTC1142 Triple Output Regulator with Switched 12V Output

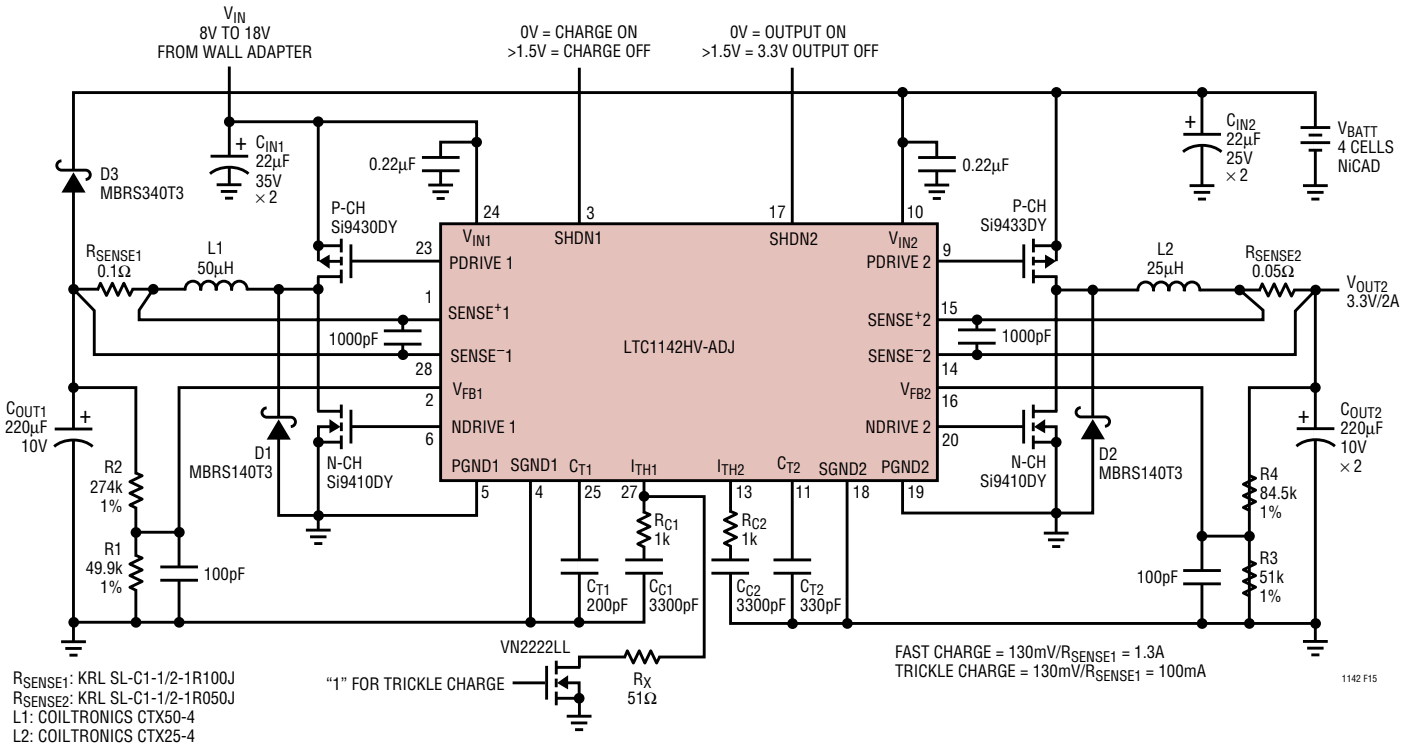


Figure 15. LTC1142HV-ADJ High Efficiency Power Supply Providing 3.3V/2A with Built-In Battery Charger

TYPICAL APPLICATIONS

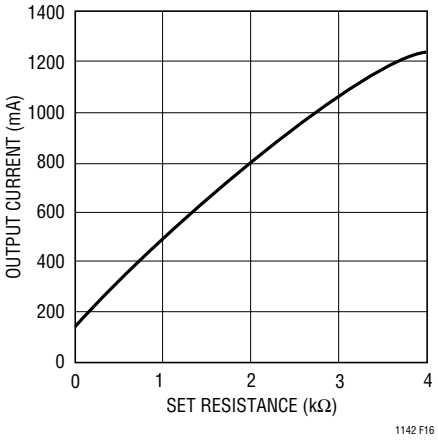
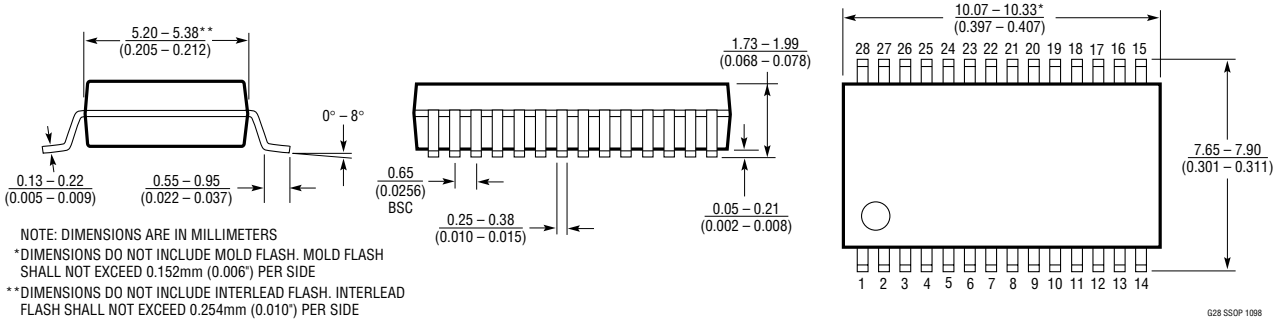


Figure 16. LTC1142HV-ADJ Output Current vs Trickle Charge Set Resistance (R_X) for the Circuit in Figure 15 Using a 0.1Ω Current Sense Resistor R_{SENSE1}

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	High Power Synchronous Step-Down Controller	SO-8 with Current Limit. No R_{SENSE} Required
LTC1625	No R_{SENSE}™ Current Mode Synchronous Step-Down Controller	Above 95% Efficiency, Needs No R_{SENSE}, 16-Lead SSOP Package Fits SO-8 Footprint
LTC1628	Dual High Efficiency 2-Phase Synch Step-Down Controller	Constant Frequency, Standby 5V and 3.3V LDOs, $3.5V \le V_{IN} \le 36V$
LTC1703	Dual 550kHz Synch 2-Phase Sw Reg Controller w/ Mobile VID	LTC1702 w/ 5-Bit Mobile VID for Mobile Pentium® Processor Systems
LTC1709	2-Phase, 5-Bit Desktop VID Synch Step-Down Controller	Current Mode, V_{IN} to 36V, I_{OUT} Up to 42A
LTC1736	Synchronous Step-Down Controller with 5-Bit Mobile VID Control	Fault Protection, PowerGood, 3.5V to 36V Input, Current Mode
LTC1753	5-Bit Desktop VID Programmable Synch Switching Reg	1.3V to 3.5V Programmable Output Using Internal 5-Bit DAC
LTC1873	Dual Synchronous Switching Regulator with 5-Bit Desktop VID	1.3V to 3.5V Programmable Core Output Plus I/O Output
LTC1929	2-Phase, Synchronous High Efficiency Converter	Current Mode Ensures Accurate Current Sensing, V_{IN} Up to 36V, I_{OUT} Up to 40A

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